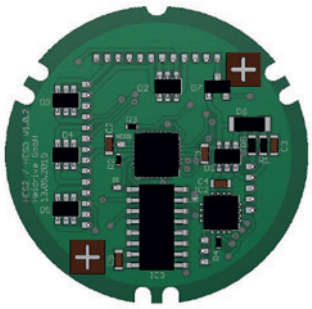
HES / HEM

Hall-Encoder

Features:



The HES / HEM encoders are designed for installation in our HeiMotion series. They are connected to the connectors on the motor side. The pin assignment can be found in the separate catalogs for the motor series. The encoders in the HES/HEM series detect a magnetic field which is generated by a magnet at the end of the shaft

Depending on the variant, the following interfaces are available:

- SSI, BiSS C (BP3) with 4096 values per revolution
- Incremental signals ABZ with 256 to 2048 PPR[3]
- Commutation signals UVW suitable for the motor
- sin/cos output with 1 period per revolution and 1 V_{PP}

Type	Absolute encoders singleturn	Absolute encoders multiturn, battery backed		Incremental and/or commutation signals	
Variant	HES1-002	HEM1-001	HEM1-002	HES2	HES3
sin/cos 1 period / revolution	differential, 1.0 V_{pp} (only with braid wire X2)			-	
SSI	SSI differential, gray coded, 12 bit ST	BiSS differential, binary coded, 20 bit MT + 12 bit ST		SSI single ended, gray coded, 12 bit ST (only with connector X1)	-
Incremental ABZ (PPR)[3]	-			differential (256)	differential (2048)
Commutation signals UVW	-			-	differential
Temperature range	- 30 °C to +125 °C				
Comment		external battery required	with built-in battery		

[1] Singleturn (ST)
[2] Multiturn (MT)
[3] Pulses Per Revolution
4 x PPR = Counts Per Revolution (CPR)

Specifications

Electrical specifications

ESD voltage (all pins)	2 kV
Power supply voltage V_{CC}	5.0 V_{DC} ± 10 %

Digital in- and outputs SSI / BiSS, ABZ, UVW		differential (RS422)	single ended (TTL)
Maximum frequency *		SSI: 4 MHz, BiSS C: 10 MHz	
Input voltage CLK+, CLK-	high	min. + 0.3 V diff.	min. 2.0 V
	low	max. - 0.3 V diff.	max. 0.8 V
Output voltage DATA+, DATA-, A+, A-, B+, B-, Z+, Z-, U+, U-, V+, V-, W+, W-	high	min. V_{CC} - 2,2 V	
	low	max. 0.4 V	
Output current (per output)		max. 50 mA	

* Can be lower depending on the connection requirements.

Analog outputs sin und cos	1.0 V_{pp} differential
Amplitude sin+, sin-, cos+, cos-	0.25 V ± 20 %
Reference level	V_{CC} / 2 ± 20 %
Periods / revolution	1
Output current (per output)	max. 50 mA

Valid norms

Norm	Safety regulations according to EN 61010-1
	Electromagnetic compatibility to EN 61000-4-3
Galvanic isolated power supply required (SELV or PELV sources)	

Heidrive Encoder Single-/ Multiturn 1 (HES 1 / HEM 1)

Variant	HES1-002	HEM1-001	HEM1-002
SSI	SSI differential	BiSS differential	
Coding	gray	binary	
Multiturn	-	20 bit / 1,048,576 revolution	
Singleturn	12 bit		
Resolution	0.088° (12 bit)		
Accuracy	typical 0.3°		
Repeatability	0.05°		
sin/cos differential	1.0 V_{pp}		
Power supply voltage	5.0 V_{DC} ± 10 %		
Current consumption (typical, without load)	25 mA	30 mA	
With 120 Ohm load and SSI Data	65 mA	70 mA	
With maximum load	175 mA	180 mA	
Battery	-	without	with TLH-2450
Standby power	-	3.0 to 5.5 V	-
Standby current	-	typical 8 µA (3.6 V)	-
Maximum speed	20,000 min^{-1}		

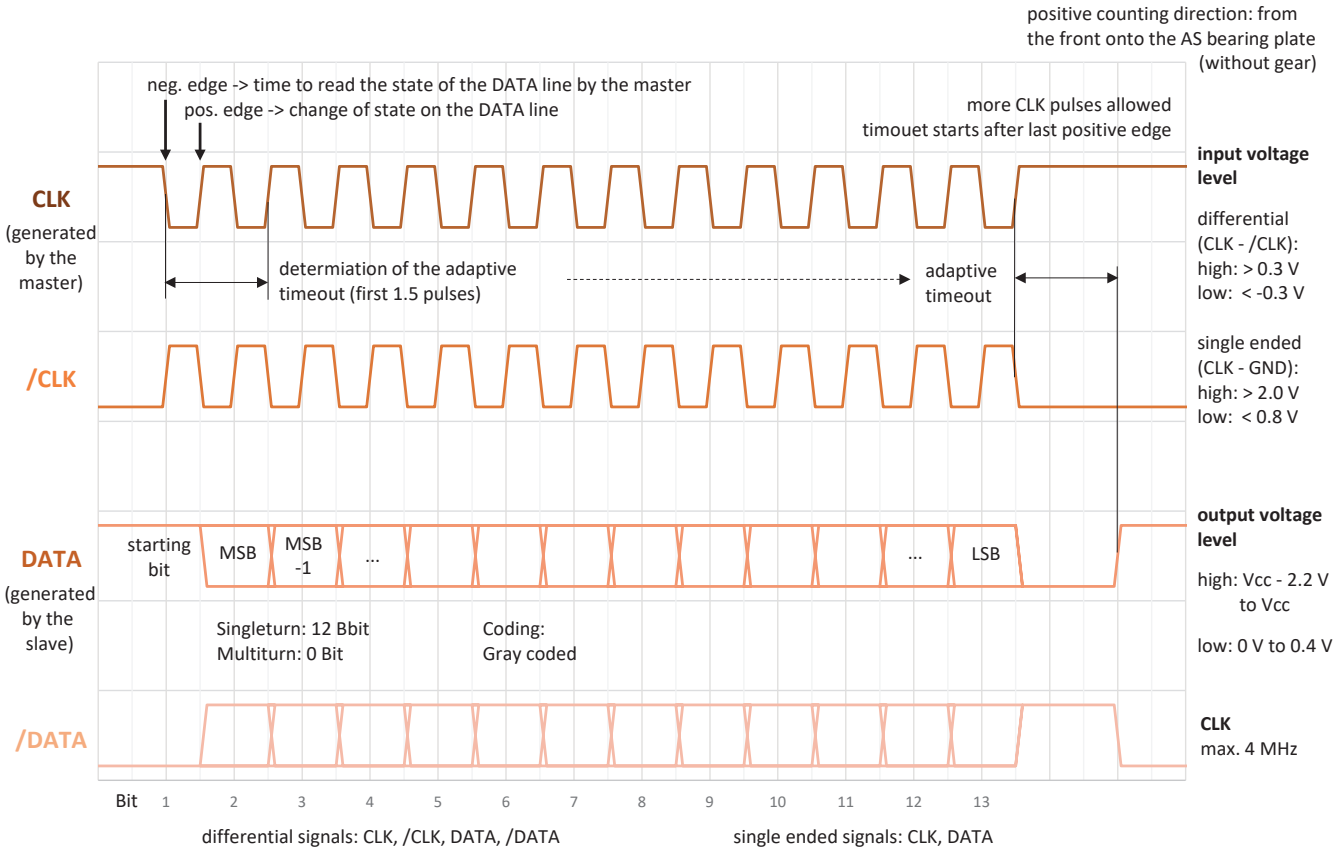
Heidrive Encoder Singleturn 2 and 3 (HES 2 / 3)

Variant	HES2	HES3
SSI	SSI single ended (only with connector X1)	-
Coding	gray	-
Singleturn	12 bit	-
ABZ (PPR)*	differential (256)	differential (2048)
Resolution	0.35°	0.044°
Accuracy	typical 0.5°	typical 0.3°
Repeatability	0.2°	0.05°
Power supply voltage	5.0 V_{DC} ± 10 %	
Current consumption (typical, without load)	25 mA	30 mA
With 120 Ohm load on ABZ and UVW	150 mA	280 mA
With maximum load	175 mA	330 mA
Maximum speed	20,000 min^{-1}	

* Pulses Per Revolution
4 x PPR = Counts Per Revolution (CPR)

SSI signal

SSI diagram

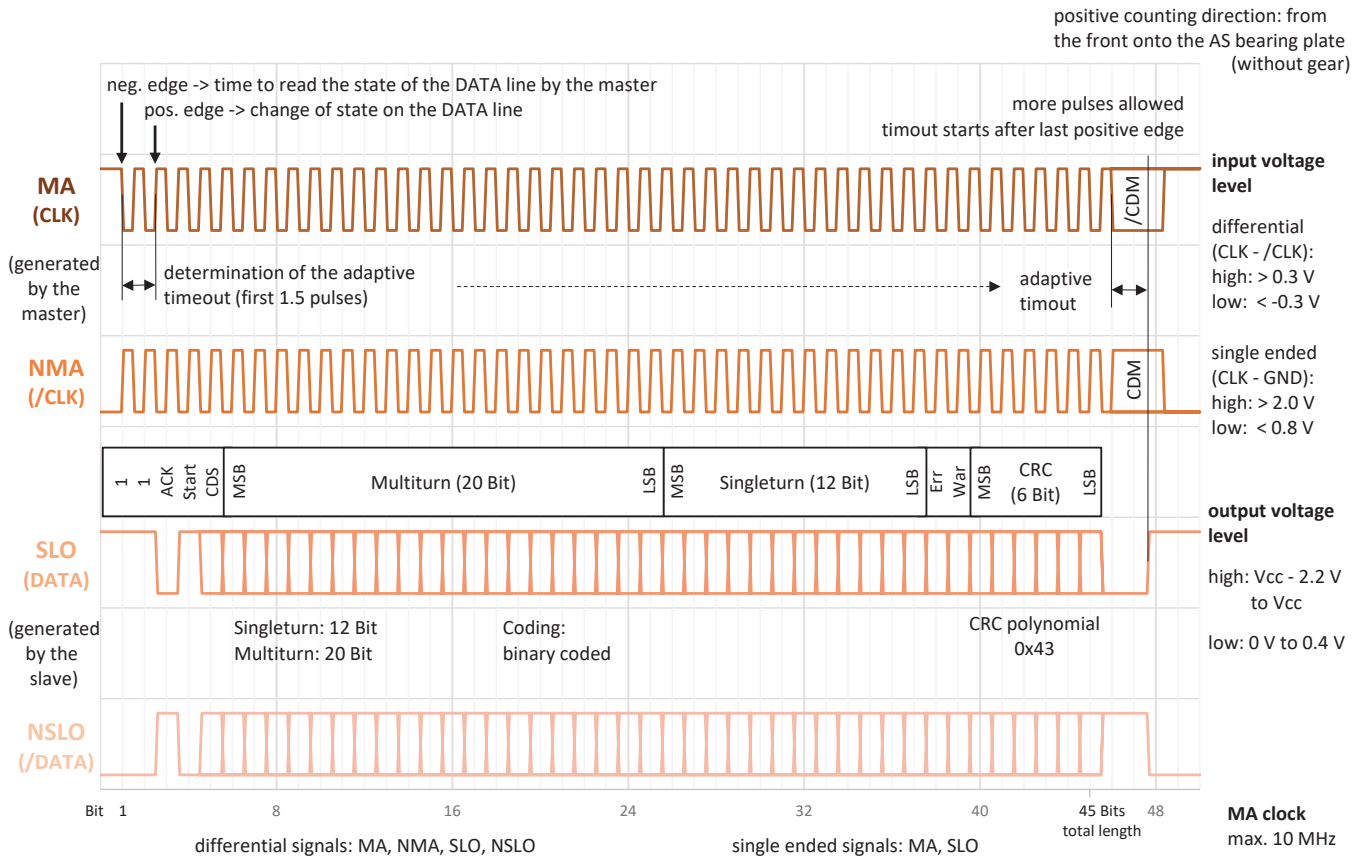


SSI signals

CLK	Clock signal, generated by the master.
/CLK	Inverted CLK signal, used for differential transmission.
DATA	Response of the encoder with the angular value, synchronous with the CLK signal of the master.
/DATA	Inverted DATA signal, used for differential transmission.
Startbit	First bit to be read, always high.
MSB	Most significant bit
LSB	Least significant bit
Adaptive timeout	The duration of the timeout is determined by the time from the first negative edge of the CLK signal to its second positive edge. After expiration of the duration of the timeout, the internal shift register of the encoder is set to 0 again. Starts with the last positive edge of the CLK signal.

BiSS signal

BiSS diagram

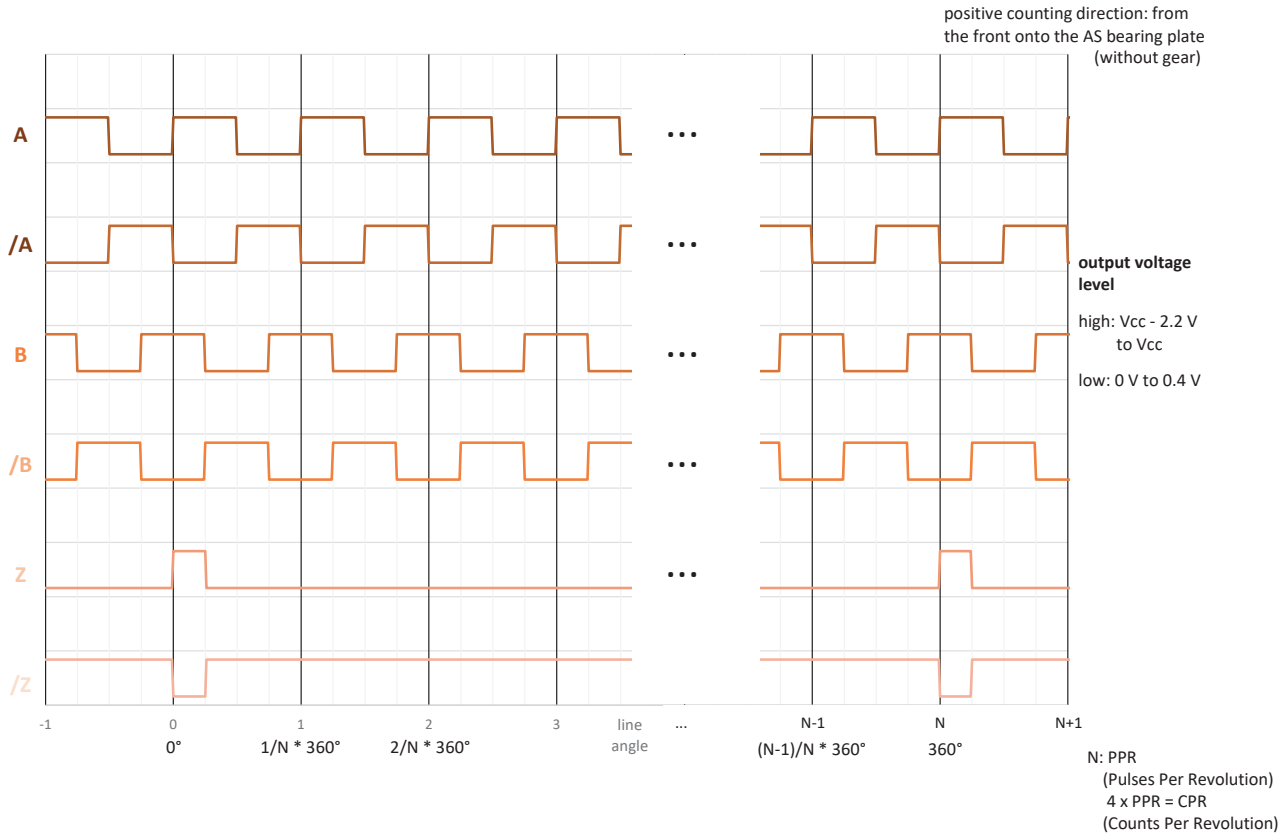


BiSS signals

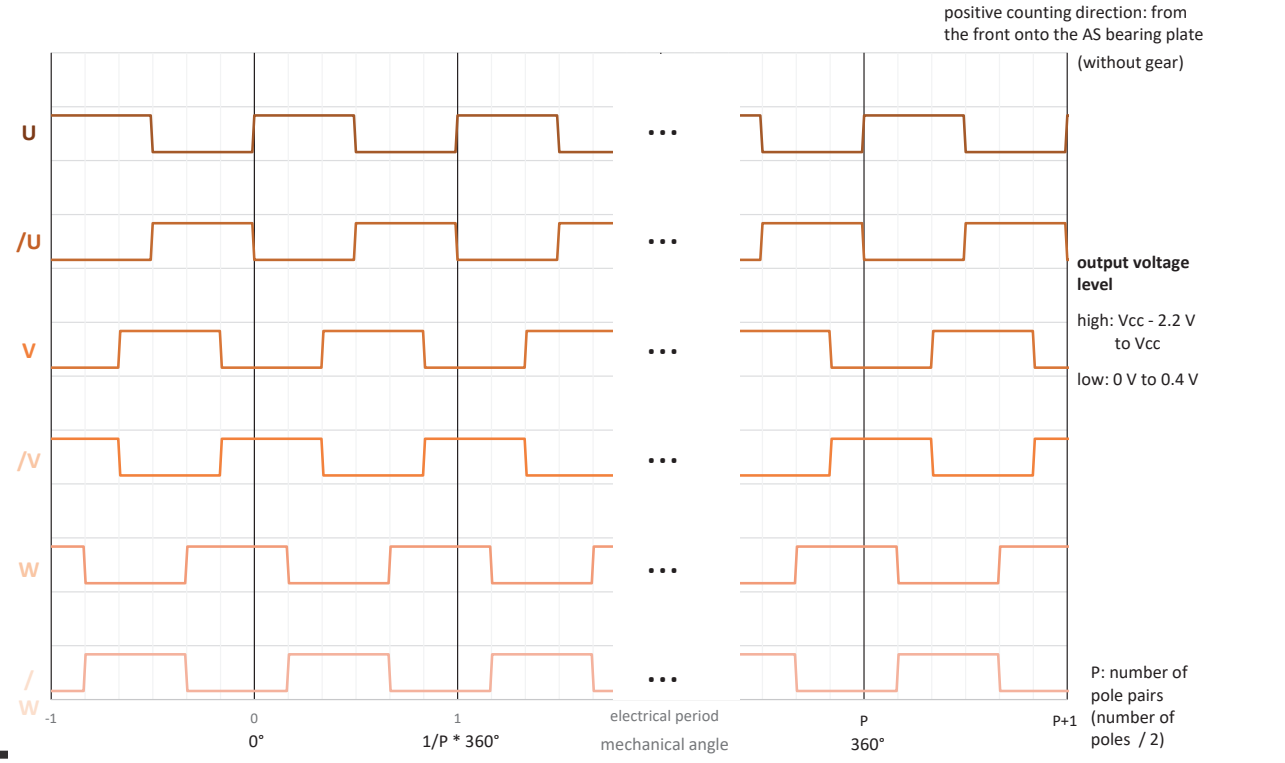
MA	Clock signal, signal generated by the master for clock-synchronous polling of the angular value (corresponds to CLK for SSI).
NMA	Inverted MA signal, used for differential transmission (corresponds to /CLK for SSI).
SLO	SLave Out, data package containing, among other things, the angular value, response of the encoder to the MA signal, synchronous with the MA signal of the master (corresponds to DATA for SSI).
NSLO	Inverted SLO signal, used for differential transmission (corresponds to /DATA for SSI)
CDM	Control Data Master, one bit per frame can be transmitted from the master to the encoder. The bit is the state of the SLO line at the moment of the timeout. The bits are composed to a BiSS command.
ACK	ACKnowledge. Response of the encoder that the transmission is ready. SLO changes from high to low on readiness.
Start	Startbit. SLO state is always high.
CDS	Control Data Slave. Response of the slave to the CDM.
MSB	Most significant bit
LSB	Least significant bit
Err	Error bit. High: encoder in error state. Low: The encoder does not show any error.
Warn	Warning bit. High: encoder shows a warning. Low: encoder shows no warning.
CRC	Cyclic Redundancy Check with polynom 0x43. Serves to monitor the transmitted data.
Adaptive timeout	The duration of the timeout is determined by the time from the first negative edge of the MA signal to its second positive edge. After expiration of the duration of the timeout, the internal shift register of the encoder is set to 0 again. Starts with the last positive edge of the MA signal.

ABZ signal, UVW signal

ABZ diagram



UVW diagram



Notes

Technical data subject to change! Last changes: 08/2024

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